4.5V-100V Vin, 1.2A, Step-down DCDC Converter

FEATURES

- Wide Input Range: 4.5V-100V
- 1.2A Continuous Output Current
- 2.75A peak current limit
- Integrated 600mΩ High-Side and 300mΩ Low-Side Power MOSFETs
- 15uA Quiescent Current with VCC diode
  160uA Quiescent Current without VCC diode
- Selectable PFM, USM and FPWM Operation Modes
- 1.2V ±2% Feedback Reference Voltage
- 4.3ms Internal Soft-start Time
- Fixed Switching Frequency at 300KHz
- COT Control Mode
- FPWM mode support Iso-buck Topology
- Precision Enable Threshold for Programmable Input Voltage Under-Voltage Lock Out Protection (UVLO) Threshold and Hysteresis
- Cycle-by-Cycle Current Limit
- Over-Voltage Protection
- Over-Temperature Protection
- Available in an ESOP-8 Package

APPLICATIONS

- GPS tracker
- E-bike, Scooter
- BMS

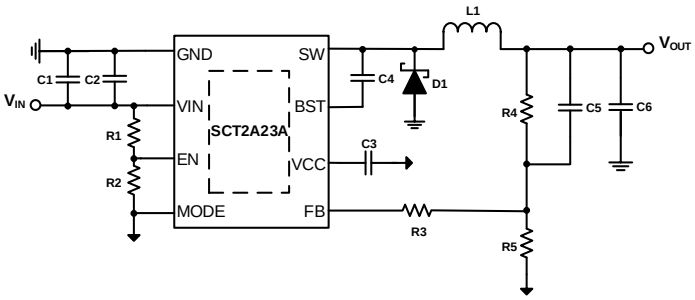
DESCRIPTION

The SCT2A23A is 1.2A Step-down DCDC converter with wide input voltage, ranging from 4.5V to 100V, which integrates an 600mΩ high-side MOSFET and a 300mΩ low-side MOSFET. The SCT2A23A, adopting the constant-on time (COT) mode control, supports the PFM mode with typical 160uA low quiescent current which assists the converter on achieving high efficiency at light load or standby condition.

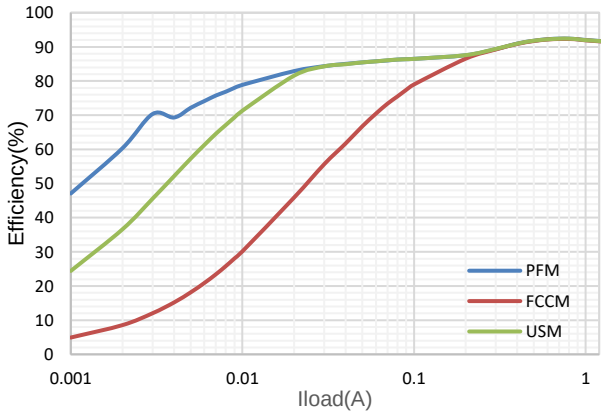
The SCT2A23A features selectable operation mode at light load, which provides the flexibility to select Pulse Frequency Modulation (PFM) to achieve high efficiency at the light-load, Ultrasonic Mode (USM) to keep the switching frequency above audible frequency areas during light-load conditions and forced Pulse Width Modulation (FPWM) to achieve smaller output ripple and support isolation buck topology.

The SCT2A23A offers cycle-by-cycle current limit protection, thermal shutdown protection, output over-voltage protection and over temperature protection. The device is available in an 8-pin thermally enhanced ESOP-8 package.

TYPICAL APPLICATION



4.5V-100V, Buck Converter



Efficiency, Vin=48V, Vout=12V

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REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

Revision 1.1: Update typo(I2) in Figure 7.

Revision 1.2: Update I_{SHDN} max value in EC.

Revision 1.3: Update DEVICE ORDER INFORMATION.

Revision 1.4: Update THERMAL INFORMATION.

DEVICE ORDER INFORMATION

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2A23ASTER	Tape & Reel	4000	A23A	8	ESOP-8

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	105	V
BOOT	-0.3	110	V
SW	-1	105	V
VCC, MODE	-0.3	30	V
BOOT-SW	-0.3	6	V
FB	-0.3	6	V
Operating junction temperature T_J(2)	-40	150	°C
Storage temperature TSTG	-65	150	°C

PIN CONFIGURATION

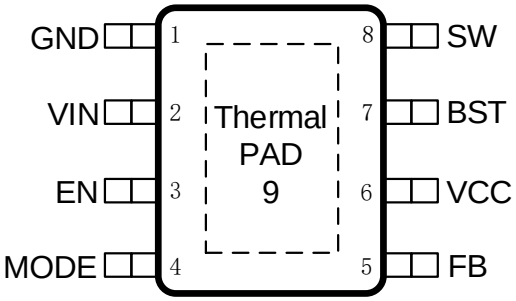


Figure 1. 8-Lead Plastic E-SOP

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

PIN FUNCTIONS

NAME	NO.	PIN FUNCTION
GND	1	Ground
VIN	2	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
EN	3	Enable pin to the regulator with internal pull-up current source. a) Float or connect to VIN to enable the converter. b) Pull below 1.23V to disable the converter. c) Resistor divider from VIN to GND connecting EN pin can adjust the input voltage lockout threshold.
MODE	4	PFM, USM and PWM mode selection. a) Connect the pin to VCC by a resistor will force the device in Forced Pulse Width Modulation (FPWM mode). b) Ground the pin to operate the device in Pulse Frequency Modulation (PFM mode) c) Floating the pin to operate the device in Ultrasonic Modulation (USM mode).

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FB	5	Inverting input of the internal PWM comparator. The tap of external feedback resistor divider from the output to GND sets the output voltage. The device regulates FB voltage to the internal reference value of 1.2V typical.
VCC	6	Output from the Internal High Voltage Regulator. The internal VCC regulator provides bias supply for the gate drivers and other internal circuitry. A larger than 1.0 μF decoupling capacitor is recommended.
BST	7	Power supply bias for high-side power MOSFET gate driver. Connect a 0.1uF capacitor from BOOT pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
SW	8	Regulator switching output. Connect SW to an external power inductor
Thermal Pad	9	Heat dissipation path of die. Electrically connection to GND pin. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	4.5	100	V
V_{OUT}	Output voltage range	1.2	30	V
T_J	Operating junction temperature	-40	125	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	-1	+1	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	-0.5	+0.5	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ESOP-8L	UNIT
$R_{\theta JA}$ (1)(2)	Junction to ambient thermal resistance	33.9	°C/W
Ψ_{JT} (2)	Junction-to-top characterization parameter	4.13	
Ψ_{JB} (2)	Junction-to-board characterization parameter	11.82	
$R_{\theta JCtop}$ (1)(2)	Junction to case thermal resistance	61.63	
$R_{\theta JB}$ (2)	Junction-to-board thermal resistance	12.32	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2A23A is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2A23A. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.
(2) Measured on JESD51-7, 4-layer PCB. The values given in this table are only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7 and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN}=48V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating input voltage		4.5		100	V
V_{CC}	V_{CC} Regulator Output			7.3		V
V_{CC_UVLO}	V_{CC} UVLO Threshold	V_{IN} rising		4.1		V
	Hysteresis			250		mV
I_{VCC_LIM}	V_{CC} internal LDO current limit	VCC short to ground		30		mA
I_{SHDN}	Shutdown current from VIN pin	EN=0, no load		3	10	μA
I_Q	Quiescent current from VIN pin	PFM mode, EN floating, no load, non-switching, BOOT-SW=5V Force VCC>8V		15		μA
		PFM mode, EN floating, no load, non- switching, BOOT-SW=5V VCC floating		160		uA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		600		mΩ
R_{DSON_L}	Low-side MOSFET on-resistance			300		mΩ
Reference and Control Loop						
V_{REF}	Reference voltage of FB	T_J=25°C	1.176	1.2	1.224	V
Enable and Soft-startup						
V_{EN_H}	Enable high threshold			1.24		V
V_{EN_L}	Enable low threshold			1.23		V
I_{EN_L}	Enable pin current	EN=0V		0.35		μA
I_{EN_H}	Enable pin current	EN=1.5V		17		uA
T_{ss}	Internal soft start time			4.3		ms
Switching Frequency Timing						
F_{SW}	Switching frequency	VOUT=12V	270	300	330	kHz
T_{OFF_MIN}	Minimum off-time	V_{IN}=12V		200		ns
Operation Mode						
V_{MD_PWM}	PWM mode input logic high threshold	VCC floating	4.65			V
V_{MD_USM}	PFM mode with USM logic threshold		1.5		3.5	V
V_{MD_PFM}	PFM mode input logic low threshold				0.5	V
Current Limit and Over Current Protection						
I_{LIM_HS}	HS MOSFET current limit		2.3	2.75	3.3	A
Izc	LS zero cross current threshold	From source to drain for PSM mode		50		mA
I_{LIM_LSROC}	LS reverse current limit	From drain to source for FCCM mode		3.4		A
Protection						
		V_{FB}/V_{REF} rising		120		%

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SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} falling		115		%
V_{UVP}	Feedback under voltage with respect to reference voltage	V_{FB}/V_{REF} rising		80		%
		V_{FB}/V_{REF} falling		75		%
T_{SD}	Thermal shutdown threshold*	T_J rising		173		°C
		Hysteresis		25		°C

*Derived from bench characterization

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TYPICAL CHARACTERISTICS

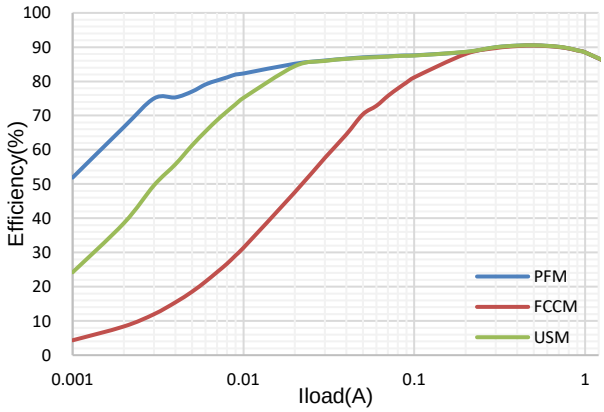


Figure 2. Efficiency, Vin=48V, Vout=12V

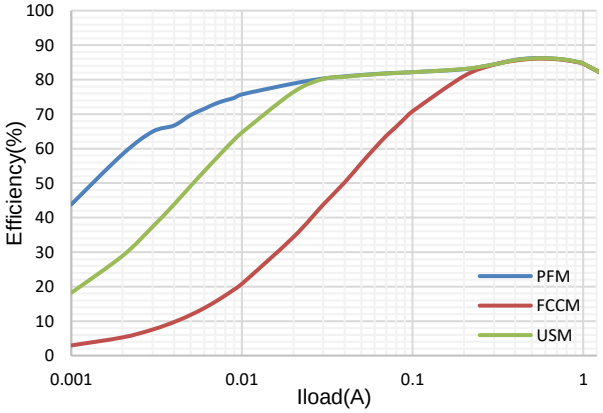


Figure 3. Efficiency, Vin=72V, Vout=12V

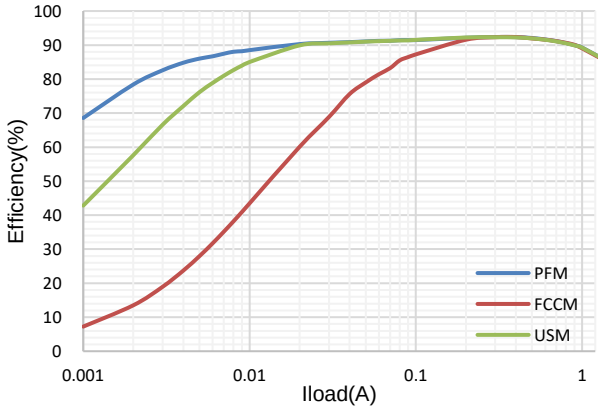


Figure 4. Efficiency with VCC diode, Vin=48V, Vout=12V

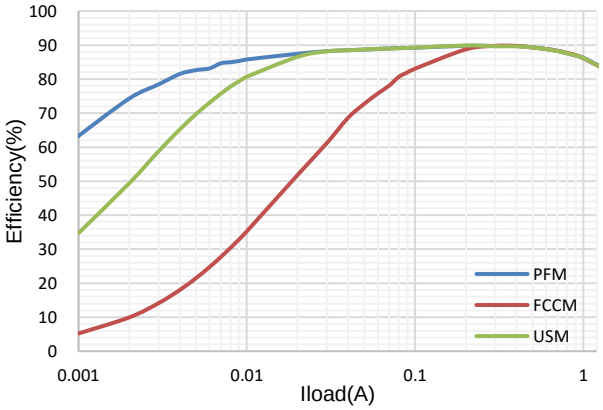


Figure 5. Efficiency with VCC diode, Vin=72V, Vout=12V

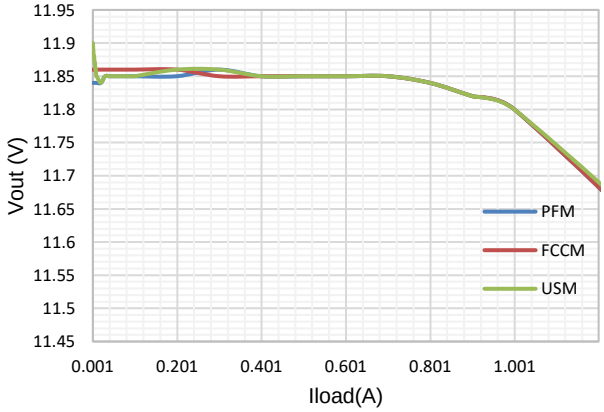


Figure 6. Load Regulation, Vin=48V, Vout=12V

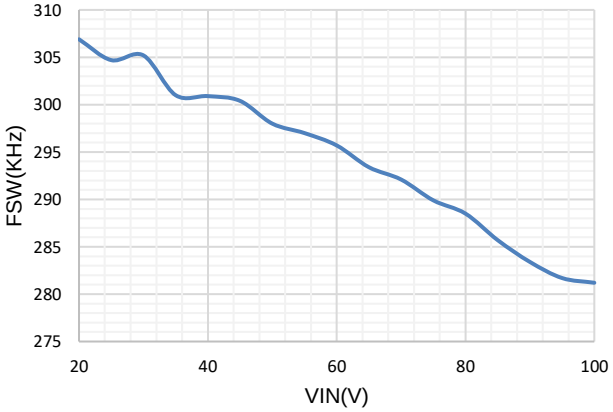


Figure 7. Switching Frequency VS Vin, Vout=12V

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FUNCTIONAL BLOCK DIAGRAM

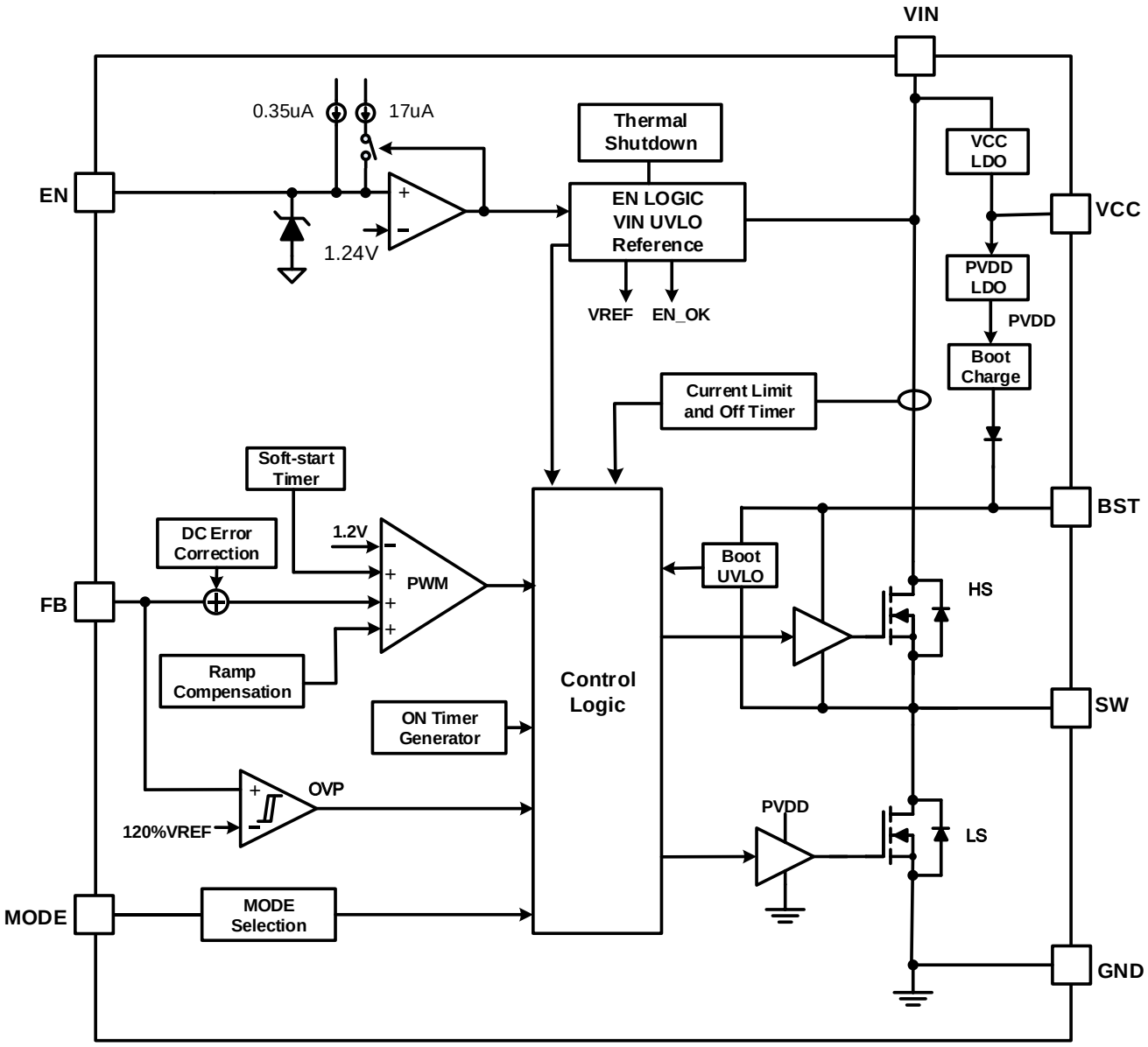


Figure 8. Functional Block Diagram

OPERATION

Overview

The SCT2A23A is a 4.5V-100V input, 1.2A output, Step-down DCDC converter with built-in 600mΩ Rdson high-side and 300mΩ Rdson low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response, and internal error amplifier also could improve the line/load regulation.

The device features three different operation modes at light loading: Pulse Frequency Modulation (PFM) mode, Ultra-Sonic Modulation (USM) mode and force Pulse Width Modulation (FPWM). In PFM mode, SCT2A23A provides high light load efficiency, because SCT2A23A design sleep control at light load for improve efficiency. In USM SCT2A23A keeps the switching frequency above audible frequency areas to avoid audible noise. In FPWM SCT2A23A achieves low output ripple and support Iso-buck topology.

The SCT2A23A features an internal 4.3ms soft-start time to avoid large inrush current and output voltage overshoot during startup. The switching frequency is fixed at 300KHz. The device also supports monolithic startup with pre-biased output condition for PSM mode and USM mode.

The SCT2A23A has a default input start-up voltage of 4.1V with 250mV hysteresis. The EN pin is a high-voltage pin with a precision threshold that can be used to adjust the input voltage lockout thresholds with two external resistors to meet accurate higher UVLO system requirements. Floating EN pin enables the device with the internal pull-up current to the pin. Connecting EN pin to VIN directly or by a resistor will start up the device automatically.

The SCT2A23A full protection features include the VCC input under-voltage lockout, the output over-voltage protection, over current protection with cycle-by-cycle current limit, output hard short protection and thermal shutdown protection.

Constant On-Time Mode Control

The SCT2A23A employs constant on-time (COT) Mode control providing fast transient with pseudo fixed switching frequency. At the beginning of each switching cycle, since the feedback voltage (VFB) is lower than the internal reference voltage (VREF), the high-side MOSFET (Q1) is turned on during one on-time and the inductor current rises to charge up the output voltage. The on-time is determined by the input voltage and output voltage. After the on-time, the high-side MOSFET (Q1) turns off and the low-side MOSFET (Q2) turns on after dead time duration. The inductor current drops and the output capacitors are discharged. When the output voltage decreases and the VFB decreased below the VREF or SS, the Q1 turns on again after another dead time duration. This repeats on cycle-by-cycle.

The SCT2A23A works with an internal compensation, so customer could use the device easily, but adding feedforward cap Cf also provides flexibility for optimizing the loop stability and transient response.

Enable and Under Voltage Lockout Threshold

The SCT2A23A is enabled when the VCC pin voltage rises about 4.1V and the EN pin voltage exceeds the enable threshold of 1.24V. The device is disabled when the VCC pin voltage falls below 3.88V or when the EN pin voltage is below 1.23V. Internal pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly or by a resistor to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R3 and R4) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

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$$VIN_rise = VEN * \frac{R3 + R4}{R4} \quad (1)$$

$$VIN_hys = I2 * R3 \quad (2)$$

Where

VIN_rise: Vin rise threshold to enable the device

VIN_hys: Vin hysteresis threshold

I_1=0.35uA : neglect in calculation

I_2=17uA

V_{EN}=1.24V, assume VEN_r = VEN_f =1.24V

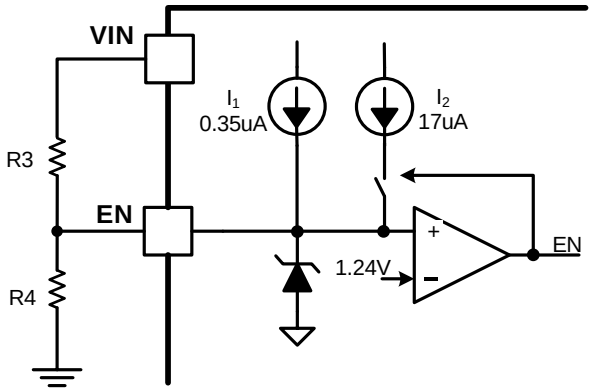


Figure 9. System UVLO by enable divide

Output Voltage

The SCT2A23A regulates the internal reference voltage at 1.2V with ±2% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$R_{FB_TOP} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_{FB_BOT} \quad (3)$$

where

- R_{FB_TOP} is the resistor connecting the output to the FB pin.
- R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2A23A integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 1.2V reference voltage in 4.3ms. If the EN pin is pulled below 1.23V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Mode Selection

The SCT2A23A features three different operation modes at light load by easily programming the MODE pin. The programming information is listed in following table. The mode setting is latched at each power up or enable and is not be able to be modified during operation.

Table 1. MODE Pin config for different operation mode

MODE Pin config	Connect to VCC by a resistor	Floating	Connect to GND
Operation Mode	FPWM	USM	PFM

Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

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Over Current Limit

The inductor current is monitored during high-side MOSFET turn on. The SCT2A23A implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current during unexpected overload or output hard short condition.

SCT2A23A also provide a HS current limit off timer for making the IC safer when trigger over current condition. Once trigger HS over current, the present on-time period is immediately terminated, and will force LS turn on a non-resettable off timer for avoiding the inductor current run away. The length of off time is controlled by FB voltage and VIN voltage and could be calculated by the following equation.

$$T_{off} = 1.5 * \left(\frac{V_{IN}}{20 * V_{FB} + 4.35}\right) us \quad (4)$$

Over voltage Protection

The SCT2A23A implements the Over-voltage Protection OVP circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When FB voltage exceeds 120% of internal 1.2V reference voltage, the high-side MOSFET turns off to avoid output voltage continue to increase, and low-side MOSFET will turn on to discharge the output voltage. When the FB pin voltage falls below 115% of the 1.2V reference voltage, the high-side MOSFET can turn on again.

Thermal Shutdown

The SCT2A23A protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 173°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 148°C, the device restarts with internal soft start phase.

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APPLICATION INFORMATION

Typical Application1

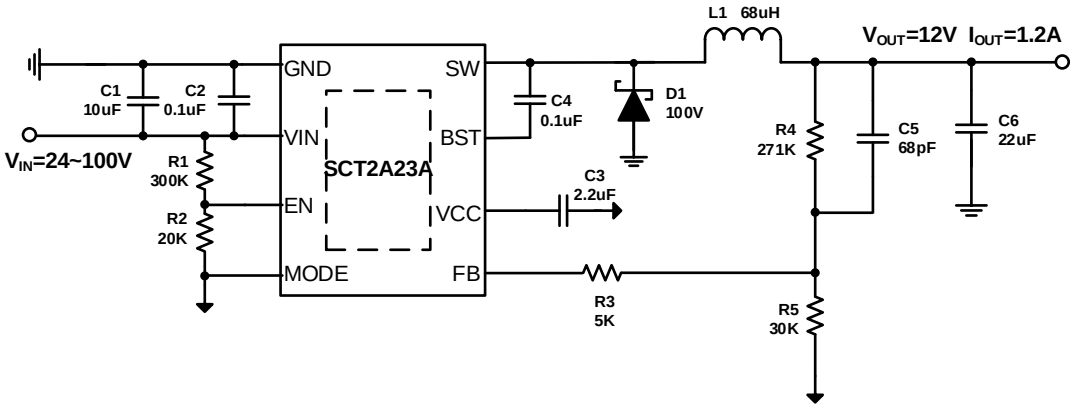


Figure 10. SCT2A23A Design Example, 12V Output with Programmable UVLO, PSM Mode

Design Parameters

Design Parameters	Example Value
Input Voltage	48V Normal， 24V to 100V
Output Voltage	12V
Output Current	1.2A
Switching Frequency	300 KHz
Output voltage ripple (peak to peak)	50mV
Transient Response 10mA to 600mA load step	ΔVout = 80mV
Transient Response 10mA to 1A load step	ΔVout = 200mV

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Typical Application2: Low Iq application

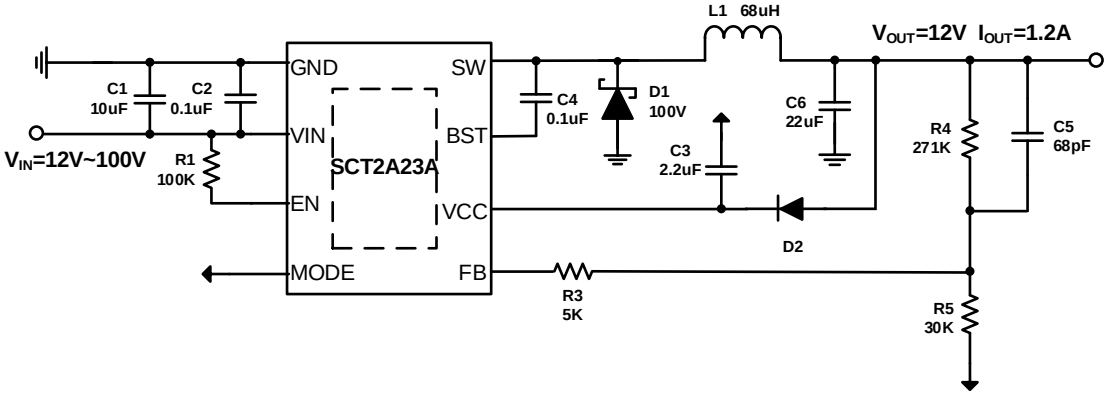


Figure 11. SCT2A23A Design Example, 12V Output with VCC diode, PSM Mode and low Iq application

Design Parameters

Design Parameters	Example Value
Input Voltage	48V Normal， 24V to 100V
Output Voltage	12V
Output Current	1.2A
Switching Frequency	300 KHz
Output voltage ripple (peak to peak)	50mV
Transient Response 10mA to 600mA load step	ΔVout = 80mV
Transient Response 10mA to 1A load step	ΔVout = 200mV

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Output Voltage

The output voltage is set by an external resistor divider R4 and R5 in typical application schematic. Recommended R5 resistance is 30KΩ. Use equation 5 to calculate R4.

$$R_4 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) * R_5 \quad (5)$$

where:

- V_{REF} is the feedback reference voltage of 1.2V

Table 2. R_1, R_2Value for Common Output Voltage (Room Temperature)

V_{OUT}	R_4	R_5
5 V	95 KΩ	30 KΩ
12V	271 KΩ	30 KΩ
24V	576 KΩ	30 KΩ

Under Voltage Lock-Out

An external voltage divider network of R_3 from the input to EN pin and R_4 from EN pin to the ground can set the input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 19.84V (start or enable). After the regulator starts switching, it should continue to do so until the input voltage falls below 14.74V (stop or disable). Use Equation 6 and Equation 7 to calculate the values 300 kΩ and 20 kΩ of R_1 and R_2 resistors.

$$VIN_{rise} = V_{EN_H} * \frac{R1 + R2}{R2} \quad (6)$$

$$VIN_hys = I2 * R1 \quad (7)$$

Where

VIN_rise: Vin rise threshold to enable the device

VIN_hys: Vin hysteresis threshold

I2=17uA

V_{EN_H}=1.24V

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 8.

$$I_{LPP} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{V_{IN} * L * f_{SW}} \quad (8)$$

Where

- I_{LPP} is the inductor peak-to-peak current
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

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Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 9 to calculate the inductance value.

$$L_{MIN} = \frac{V_{OUT}}{f_{SW} * LIR * I_{OUT(max)}} * (1 - \frac{V_{OUT}}{V_{IN(max)}}) \quad (9)$$

Where

- L_{MIN} is the minimum inductance required
- f_{sw} is the switching frequency
- V_{OUT} is the output voltage
- $V_{IN(max)}$ is the maximum input voltage
- $I_{OUT(max)}$ is the maximum DC load current
- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 10 and equation 11.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (10)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{1}{12} * (I_{LPP})^2} \quad (11)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 2.75A. The most conservative approach is to choose an inductor with a saturation current rating greater than 2.75A. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the SCT2A23A can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Diode Selection

The SCT2A23A requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN(max). The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. A diode with a minimum of 100-V reverse voltage is preferred to allow input voltage transients up to the rated voltage of the SCT2A23A.

For the example design, the SS510 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the SS510 is 0.7 volts at 5 A.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, the ac losses of the diode need to be taken into account. The ac losses of the diode are due to the

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charging and discharging of the junction capacitance and reverse recovery charge. Equation 12 is used to calculate the total power dissipation, including conduction losses and ac losses of the diode.

The SS510 diode has a junction capacitance of 300 pF. Using Equation 12, the total loss in the diode at the maximum input voltage is 1.24 W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{(V_{IN_MAX} - V_{OUT}) \times I_{OUT} \times V_d}{V_{IN_MAX}} + \frac{C_j \times f_{SW} \times (V_{IN} + V_d)^2}{2} \quad (12)$$

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 13.

$$I_{CINRMS} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})} \quad (13)$$

The worst case condition occurs at V_{IN}=2*V_{OUT}, where:

$$I_{CINRMS} = 0.5 * I_{OUT} \quad (14)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 15 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} * C_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}}) \quad (15)$$

For this example, one 10μF, X7R ceramic capacitors rated for 100 V in parallel are used. And a 0.1 μF for high-frequency filtering capacitor is placed as close as possible to the device pins.

Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between BOOT pin and SW pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

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The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 16 desired.

$$\Delta V_{OUT} = \frac{V_{OUT} * (V_{IN} - V_{OUT})}{8 * f_{SW}{}^2 * L * C_{OUT} * V_{IN}} \quad (16)$$

Where

- $\Delta V_{OUT}$is the output voltage ripple
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- $V_{IN}$is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 22μF ceramic output capacitors work for most applications.

Table 3 lists typical values of external components for some standard output voltages.

Table 3: Component List with Typical Output Voltage BOM list

Vout	L1	COUT	R4	R5	C5
5V	33uH	2*22uF	95K	30K	68pF
12V	68uH	2*22uF	271K	30K	150pF
24V	100uH	2*22uF	576k	30K	220pF

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Application Waveforms

Vin=48V, Vout=12V, unless otherwise noted

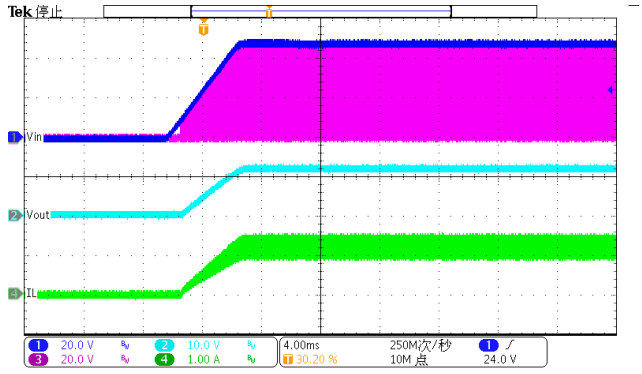


Figure 12. Power up (Iload=2A)

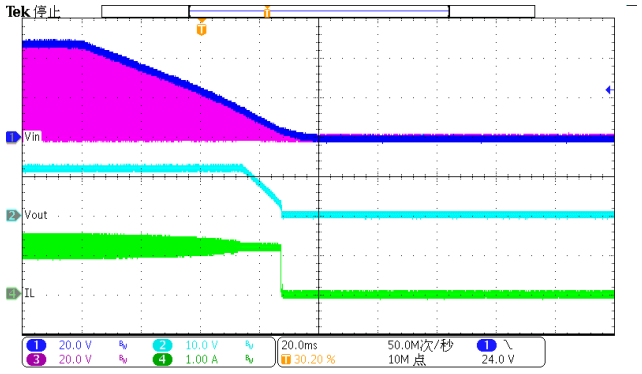


Figure 13. Power down (Iload=1.2A)

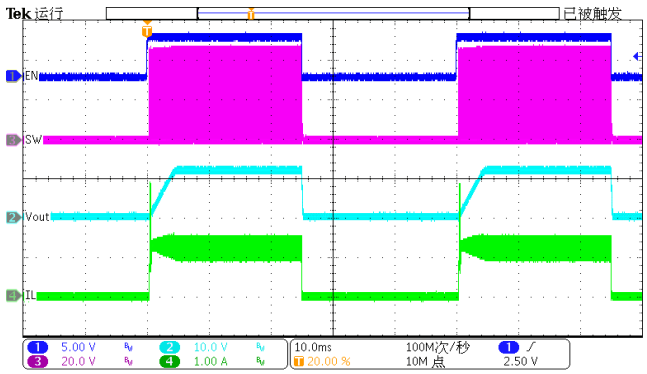


Figure 14. Enable toggle Iload=1.2A)

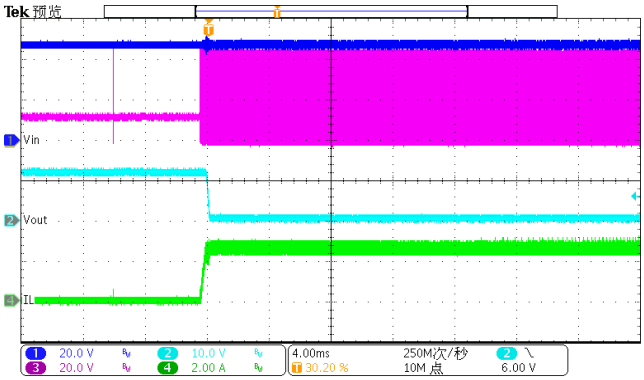


Figure 15. Output Hard Short Protection

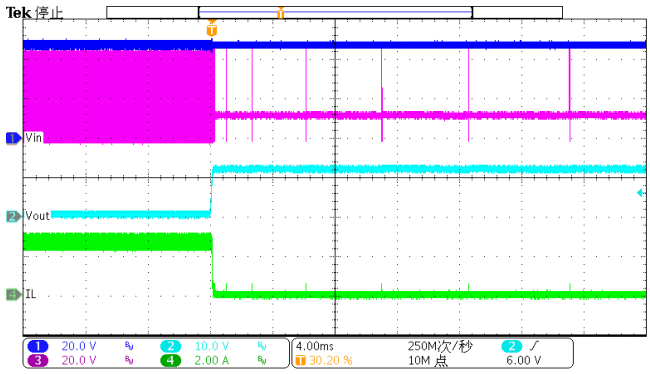


Figure 16. Output Hard Short Release

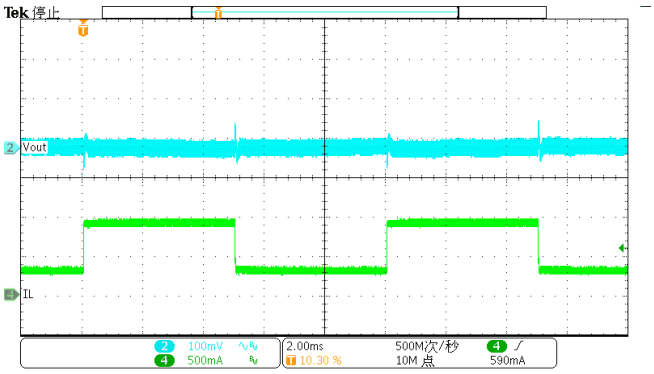


Figure 17. Load Transient (0.3A to 0.9A, 1.6A/us)

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Application Waveforms (Continued)

Vin=48V, Vout=12V, unless otherwise noted

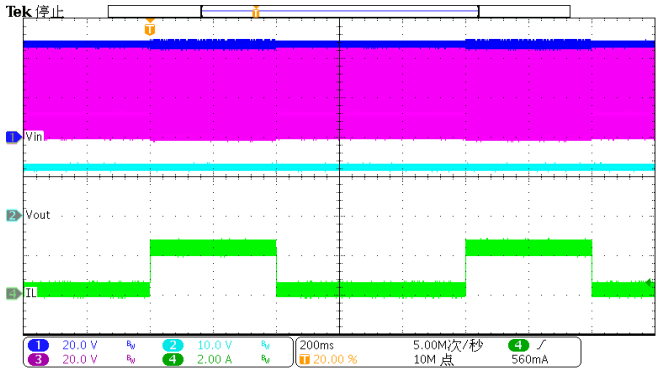


Figure 18. Load Transient 0A to 2.3A (400ms)

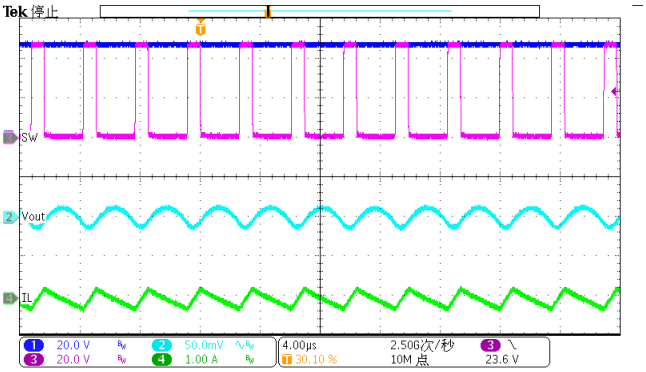


Figure 19. Output Ripple (Iload=0A, FCCM)

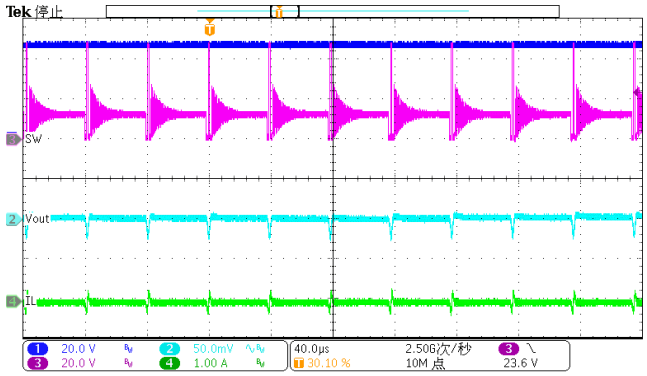


Figure 20. Output Ripple (Iload=0A, USM)

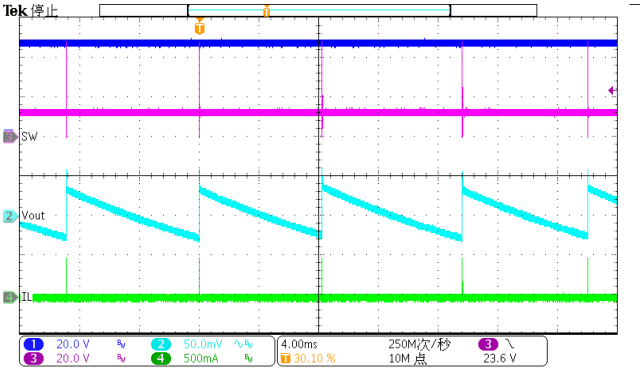


Figure 21. Output Ripple (Iload=0A, PFM)

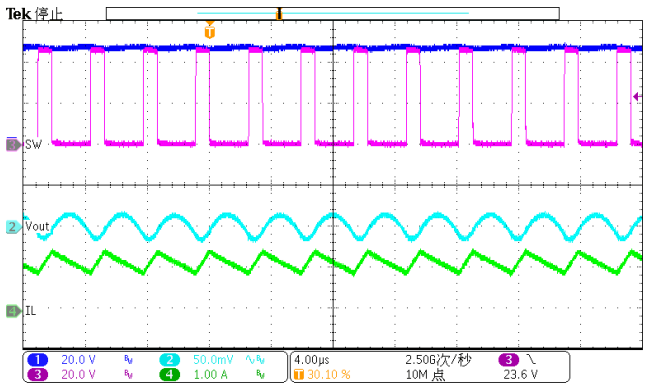


Figure 22. Output Ripple (Iload=1.2A)

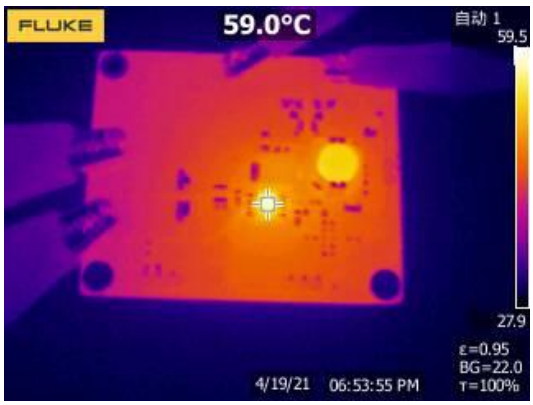


Figure 23. Thermal, 48VIN, 12Vout, 1.2A

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Typical Application3: Iso-Buck Application

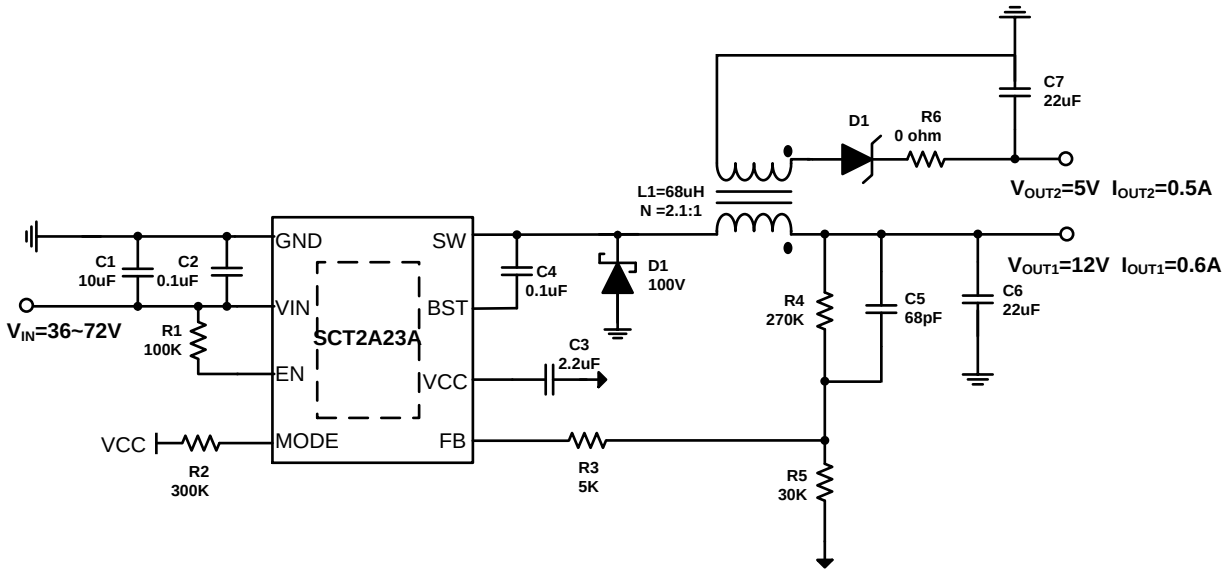


Figure 24. SCT2A23A Design Example, Iso-BUCK application with 5V isolation Output

Design Parameters

Design Parameters	Example Value
Input Voltage	48V Normal， 36V to 72V
Output Voltage	12V/5V
Maximum Output Current	Iout1=0.6A/Iout2=0.5A
Voltage drop of VD1	0.7V
Inductor /Transformer Turns Ratio (N)	L1=68uH /N=2.1:1
Switching Frequency	300 KHz

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Design of Iso-BUCK

Selection of VOUT and Turns Ratio

The primary output voltage in a Iso-Buck converter should be no more than one half of the minimum input voltage. For example, at the minimum V_{IN} of 36 V, the primary output voltage (V_{OUT1}) should be no higher than 18V. The isolated output voltage VOUT2 is set by selecting a transformer with a turns ratio (N_1:N_2 = N_{PRI}:N_{SEC}). Using this turns ratio, the required primary output voltage V_{OUT1} is calculated by the following equation:

$$Vout1 = \frac{Vout2 + Vd1}{N2/N1} \quad (17)$$

The 0.7 V (Vd1) represents the forward voltage drop of the secondary rectifier diode. By setting the primary output voltage V_{OUT1} by selecting the correct feedback resistors, the secondary voltage is regulated at V_{OUT2} nominally. Adjustment of the primary side V_{OUT1} may be required to compensate for voltage errors due to the leakage inductance of the transformer, the resistance of the transformer windings, the diode drop in the power path on the secondary side.

Secondary Rectifier Diode

The secondary side rectifier diode must block the maximum input voltage reflected at secondary side switch node. The minimum diode reverse voltage V_{RD1} rating is given below

$$V_{RD1} = (V_{IN(max)} - Vout1) * \frac{N2}{N1} + Vout2 \quad (18)$$

A diode with higher reverse voltage rating must be selected in this application. If the input voltage (V_{IN}) has transients above the normal operating maximum input voltage, then the worst-case transient input voltage must be used in calculation while selecting the secondary side rectifier diode.

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Iso-Buck Application Waveforms

Vin=48V, Vout=12V, Viso=5V, unless otherwise noted

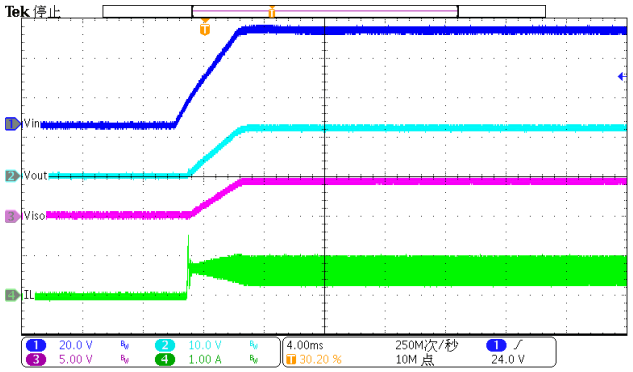


Figure 25. Power up(Io=0.6A,Iiso=0.5A)

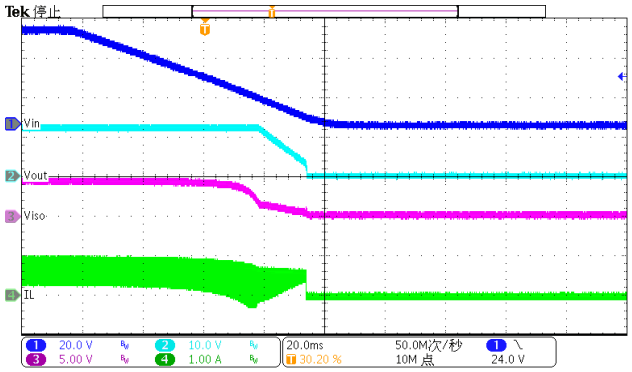


Figure 26. Power down(IO=0.6A,Iiso=0.5A)

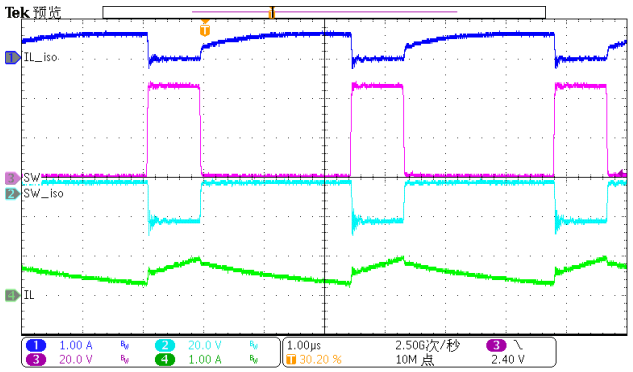


Figure 27. Steady State(Io=0.6A,Iiso=0.5A)

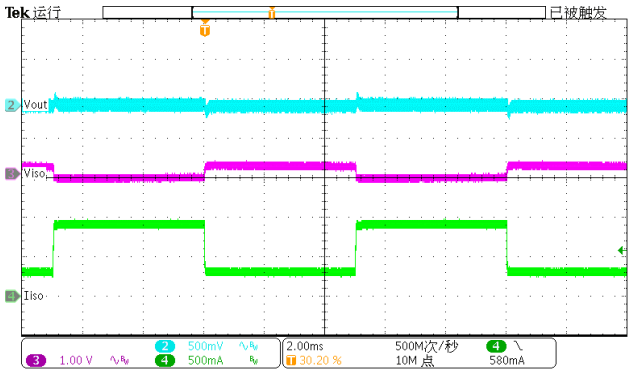


Figure 28. Load Transient 0.3A to 0.9A (isoload)

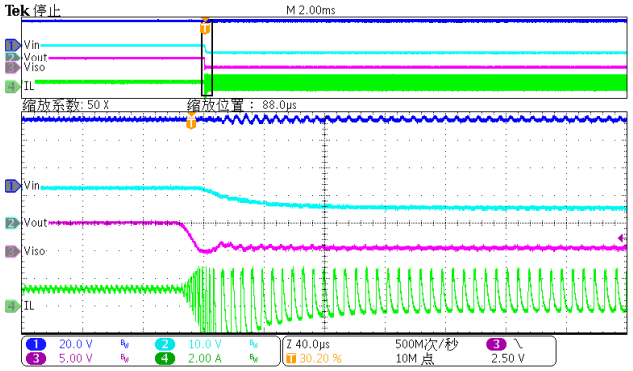


Figure 29. Secondary-Side Short(Io=1.2A)

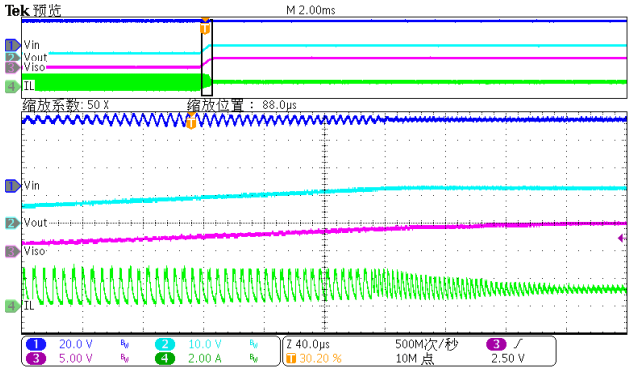


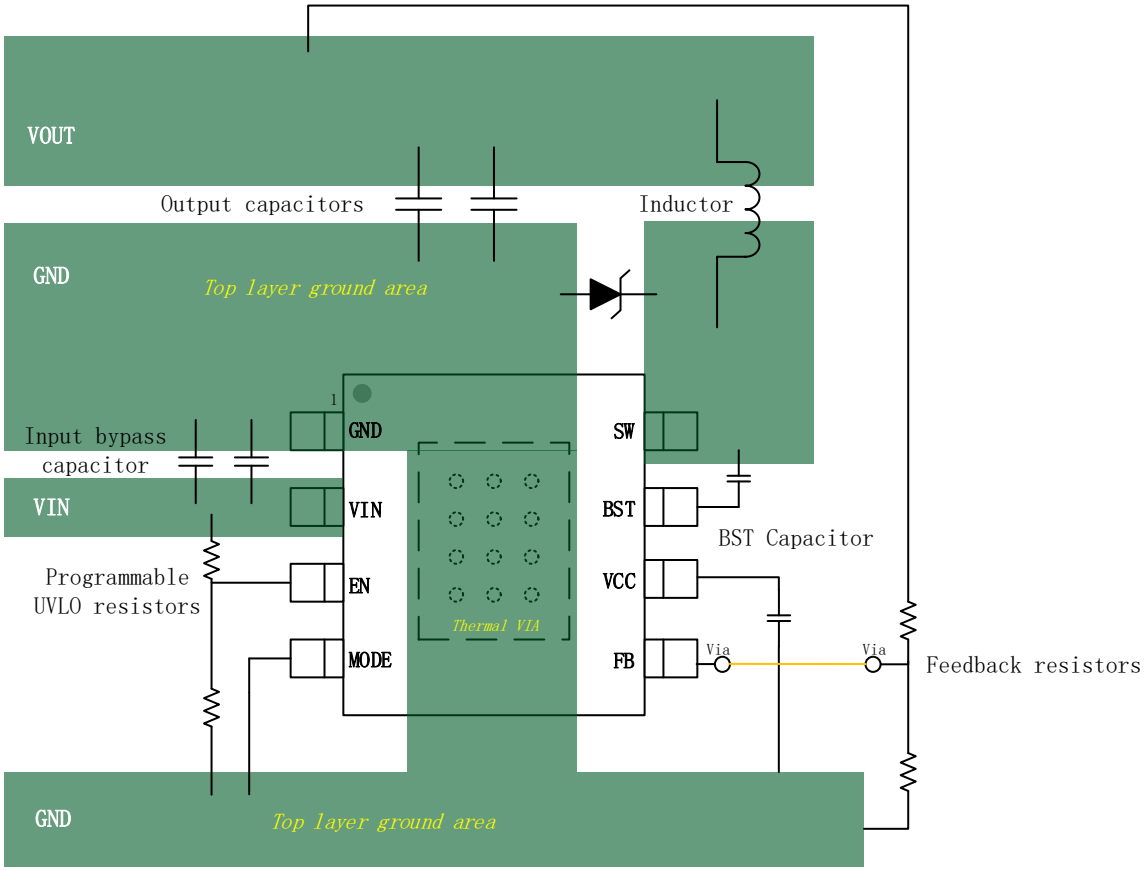
Figure 30. Secondary-Side Short Release (Io=1.2A)

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Layout Guideline

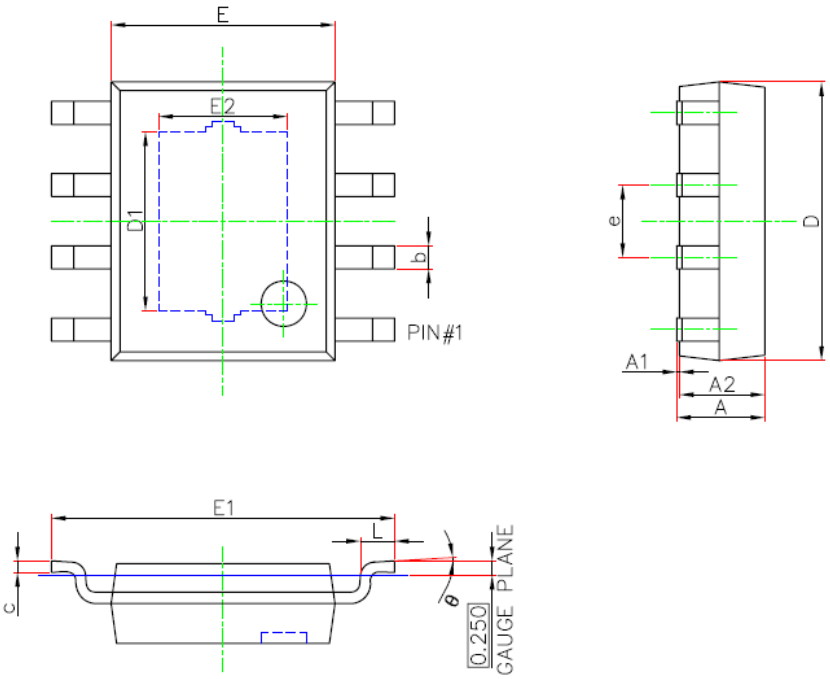
Proper PCB layout is a critical for SCT2A23A's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC. The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. It is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
5. Output inductor should be placed close to the SW pin. The area of the PCB conductor minimized to prevent excessive capacitive coupling.
6. UVLO adjust, VCC capacitor and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
7. For achieving better thermal performance, a four-layer layout is strongly recommended.



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PACKAGE INFORMATION



ESOP8/PP(95x130) Package Outline Dimensions

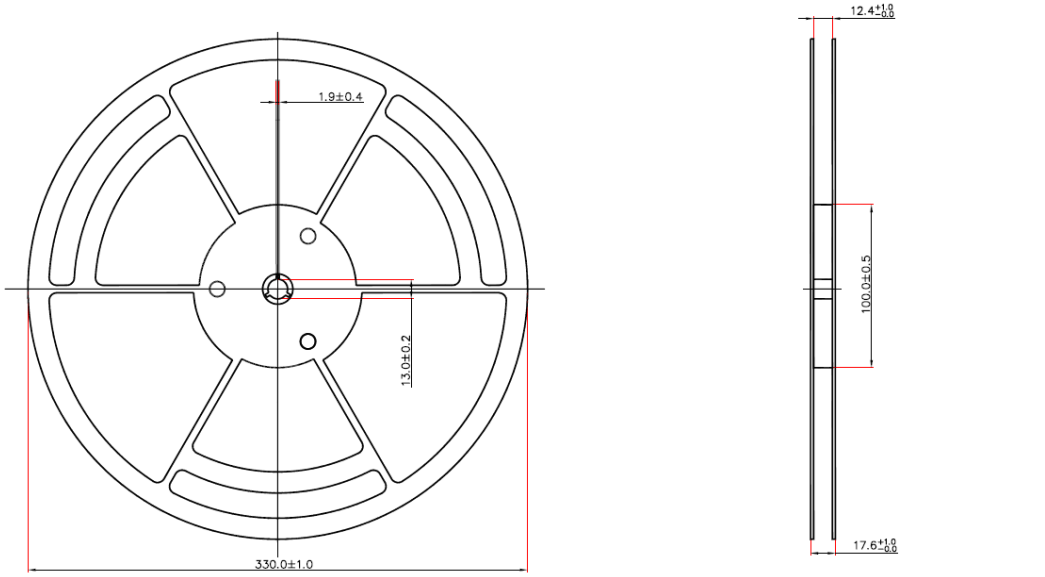
Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

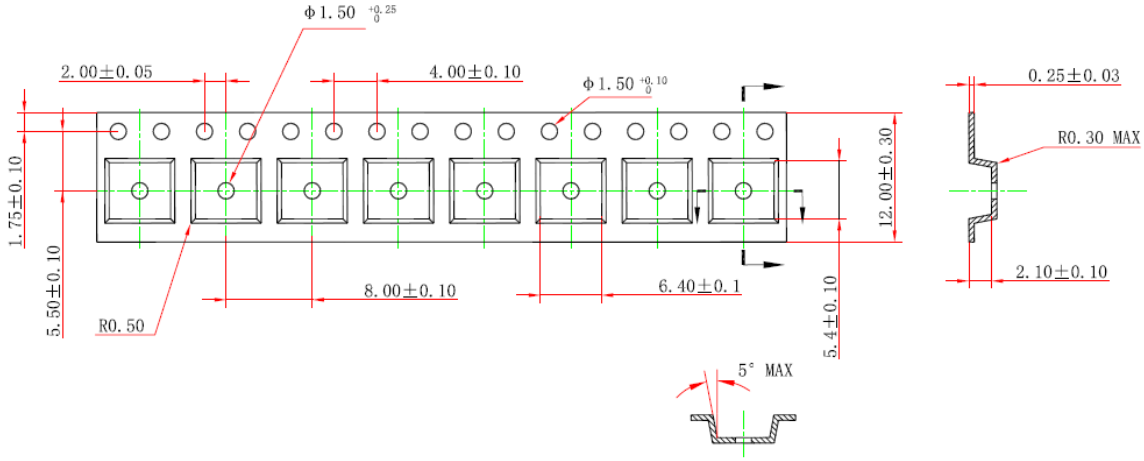
NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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TAPE AND REEL INFORMATION





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