# 17V Vin, 3A Synchronous Step-down DCDC Converter

## FEATURES

- Wide Input Voltage: 4.2-17V
- 3A Continuous Output Current with Integrated 75mΩ/45mΩ FETs
- Wide Output Voltage Range:0.8V-7V
- Quiescent Current 150uA
- Cycle-by-Cycle Current Limiting
- Internal 2.5ms Soft-Start Limits the inrush current
- Fixed 750kHz Switching Frequency
- Input Under-Voltage Lockout
- Power save mode at light load
- Over-Temperature Protection
- Available in a TSOT23-6L Package

## APPLICATIONS

- Flat Panel Digital TV and Monitors
- Surveillance
- Set Top Boxes
- Networking Systems
- Consumer Electronics
- General Purpose

## DESCRIPTION

The SCT2230 is a fully integrated high efficiency synchronous step-down DCDC converter capable of delivering 3A current. The devices operate over a wide input voltage range from 4.2V to 17V and fully integrate high-side power MOSFETs and synchronous MOSFETs with very low Rdson to minimize the conduction loss.

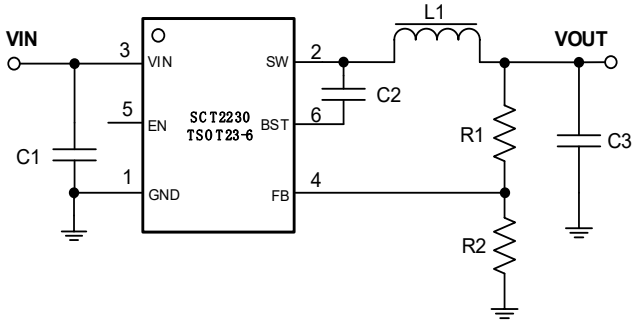
With 750 kHz switching frequency, low output voltage ripple, small external inductor and capacitor size are achieved. SCT2230 adopts adaptive constant ON-time control architecture to achieve fast load transient responses for step-down applications.

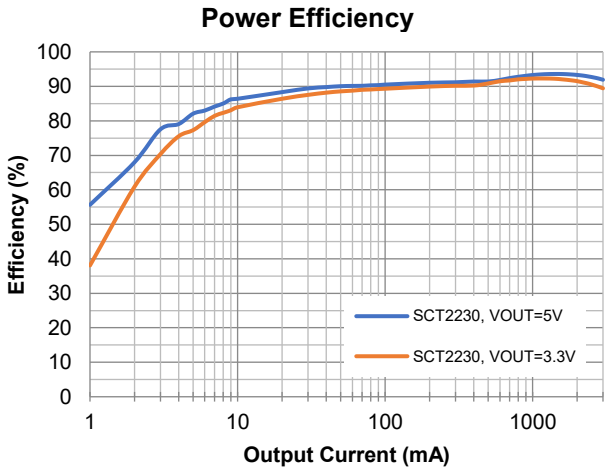
The SCT2230 operates in power saving mode, which maintains high efficiency during light load operation.

It includes full protection features, such as over current protection, output under-voltage protection, input under-voltage lockout, and thermal shutdown.

The SCT2230 requires a minimal number of external components and is available in a space-saving TSOT23-6L package.

## TYPICAL APPLICATION




 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved 

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.2: Update DEVICE ORDER INFORMATION

Revision 1.3: Update ABS TJ max and internal soft-start time in FEATURES, add MSL information, and remove information related to SCT2230TVAR

## DEVICE ORDER INFORMATION

| ORDERABLE DEVICE | PACKAGING TYPE | STANDARD PACK QTY | PACKAGE MARKING | PINS | PACKAGE DESCRIPTION | MSL |
|---|---|---|---|---|---|---|
| SCT2230TVBR | Tape & Reel | 3000 | 2230 | 6 | TSOT23-6L | 1 |

## ABSOLUTE MAXIMUM RATING

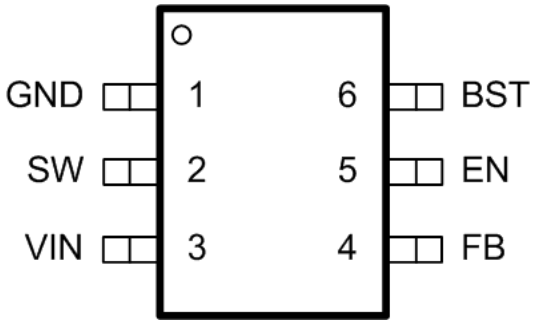
Over operating free-air temperature unless otherwise noted(1)

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $V_{IN}$ | Supply Voltage | -0.3 to 20 | V |
| $V_{SW}$ | Switch Node Voltage | -1 to VIN+0.3 | V |
| $V_{BST}$ | Bootstrap | $V_{SW}$-0.3 to $V_{SW}$+6 | V |
| $V_{FB}$ | Feedback Voltage | -0.3 to 6.5 | V |
| $V_{EN}$ | Enable/UVLO Voltage | -0.3 to 6.5 | V |
| $T_J$ | Operating junction temperature(2) | -40 to 150 | C |
| $T_{STG}$ | Storage temperature | -65 to 150 | C |

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.

(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime

## PIN CONFIGURATION




TSOT23-6L Top View
(2.8mm x 2.8mm)

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

## PIN FUNCTIONS

| NAME | PIN | PIN FUNCTION |
|---|---|---|
| GND | 1 | Power ground. Must be soldered directly to ground plane. |
| SW | 2 | Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BST to power the high-side switch. |
| VIN | 3 | Power supply input. VIN supplies the power to the IC, as well as the step-down converter switches. Drive VIN with a 4.2V to 17V power source. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC. See Input Capacitor. |
| FB | 4 | Buck converter output feedback sensing voltage. Connect a resistor divider from VOUT to FB to set up output voltage. The device regulates FB to the internal reference of 0.8V typical. |
| EN | 5 | Enable logic input. Floating the pin enables the device. Connect 100K resistor to VIN to enable the device. The device has precision enable thresholds 1.18V rising / 1.1V falling for programmable UVLO threshold and hysteresis. |
| BST | 6 | Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node. |

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 4.2 | 17 | V |
| $T_J$ | Operating junction temperature | -40 | 125 | °C |

## ESD RATINGS

| PARAMETER | DEFINITION | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1) | -2 | +2 | kV |
| | Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014specification, all pins(1) | -0.5 | +0.5 | kV |

(1) HBM and CDM stressing are done in accordance with the ANSI/ESDA/JEDEC JS-001-2014 specification

## THERMAL INFORMATION

| PARAMETER | THERMAL METRIC | TSOT23-6L | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction to ambient thermal resistance(1) | 88 | °C/W |
| $R_{\theta JC}$ | Junction to case thermal resistance(1) | 12 | |

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2230 are mounted, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2230. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

## ELECTRICAL CHARACTERISTICS

$V_{IN}$=12V, $T_J$=-40°C~125°C, typical values are tested under 25°C.

| SYMBOL | PARAMETER | TEST CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply and Output** | | | | | | |
| $V_{IN}$ | Operating input voltage | | 4.2 | | 17 | V |
| $V_{IN_UVLO}$ | Input UVLO<br>Hysteresis | $V_{IN}$ rising | | 4.0<br>300 | 4.15 | V<br>mV |
| $I_{SD}$ | Shutdown current | EN=0, No load, VIN=12V | | 1.5 | 5 | uA |
| $I_Q$ | Quiescent current | EN=2V, No load, No switching. VIN=12V. BST-SW=5V | | 155 | | uA |
| **Enable, Soft Start and Working Modes** | | | | | | |
| $V_{EN_H}$ | Enable high threshold | | | 1.18 | 1.25 | V |
| $V_{EN_L}$ | Enable low threshold | | 1.03 | 1.1 | | V |
| $I_{EN}$ | Enable pin input current | EN=1V | 1 | 1.5 | 2 | uA |
| $I_{EN_HYS}$ | Enable pin hysteresis current | EN=1.5V | | 6.8 | | uA |
| **Power MOSFETs** | | | | | | |
| $R_{DSON_H}$ | High side FET on-resistance | | | 75 | | mΩ |
| $R_{DSON_L}$ | Low side FET on-resistance | | | 45 | | mΩ |
| **Feedback and Error Amplifier** | | | | | | |
| $V_{FB}$ | Feedback Voltage | | 0.78 | 0.8 | 0.82 | V |
| **Current Limit** | | | | | | |
| $I_{LIM_LSD}$ | LSD valley current limit | | 3.2 | 3.7 | 4.2 | A |
| **Switching Frequency** | | | | | | |
| $F_{SW}$ | Switching frequency | $V_{IN}$=12V, $V_{OUT}$=5V | | 750 | | kHz |
| $t_{ON_MIN}$ | Minimum on-time | | | 90 | | ns |
| $t_{OFF_MIN}$ | Minimum off-time | | | 220 | | ns |
| **Soft Start Time** | | | | | | |
| $t_{SS}$ | Internal soft-start time | | | 2.5 | | ms |
| **Protection** | | | | | | |
| $T_{SD}$ | Thermal shutdown threshold<br>Hysteresis | $T_J$ rising | | 160<br>20 | | °C |

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

## TYPICAL CHARACTERISTICS

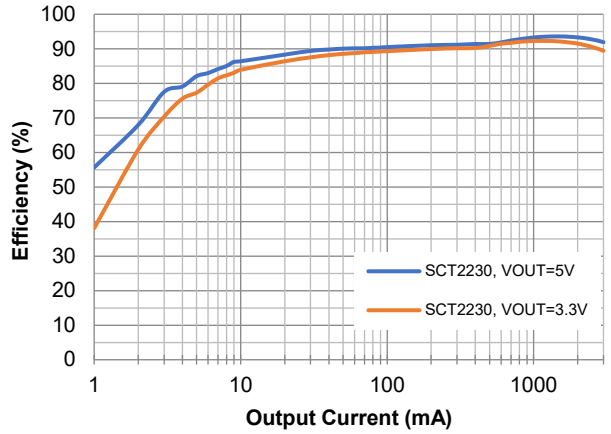



Figure 1. SCT2230 Efficiency, Vin=12V

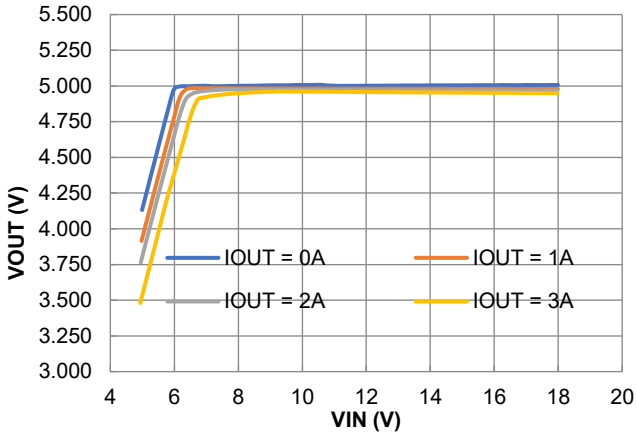



Figure 2. VOUT Vs. VIN

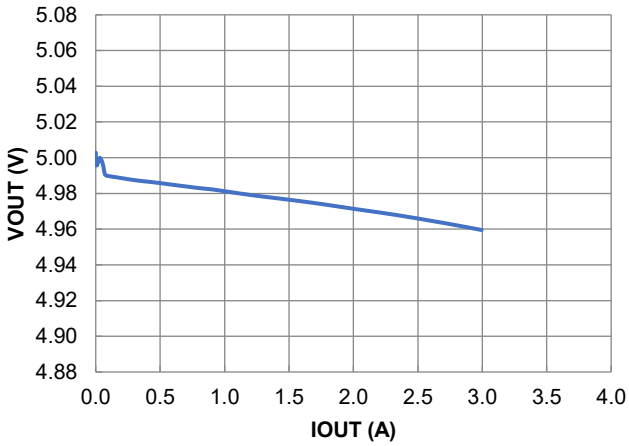



Figure 3. Load Regulation

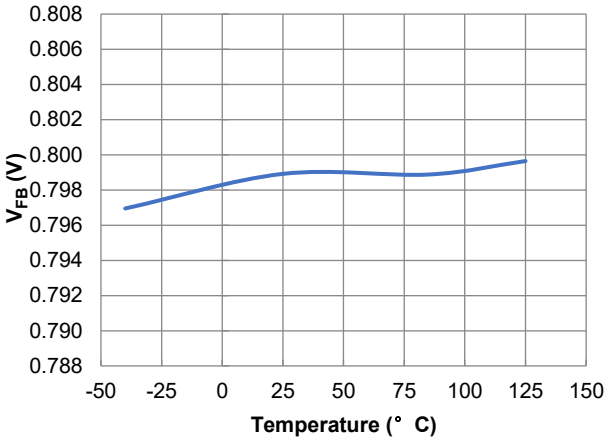



Figure 4. FB Voltage Vs. Temperature

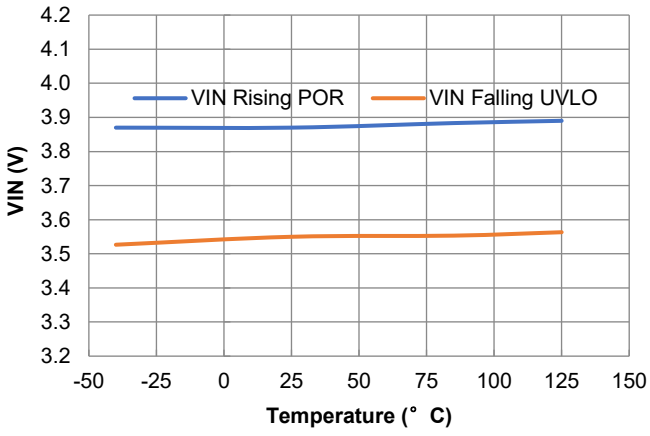



Figure 5. UVLO Vs. Temperature

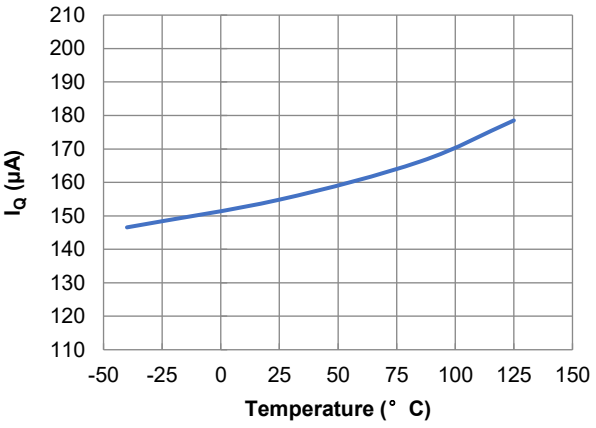
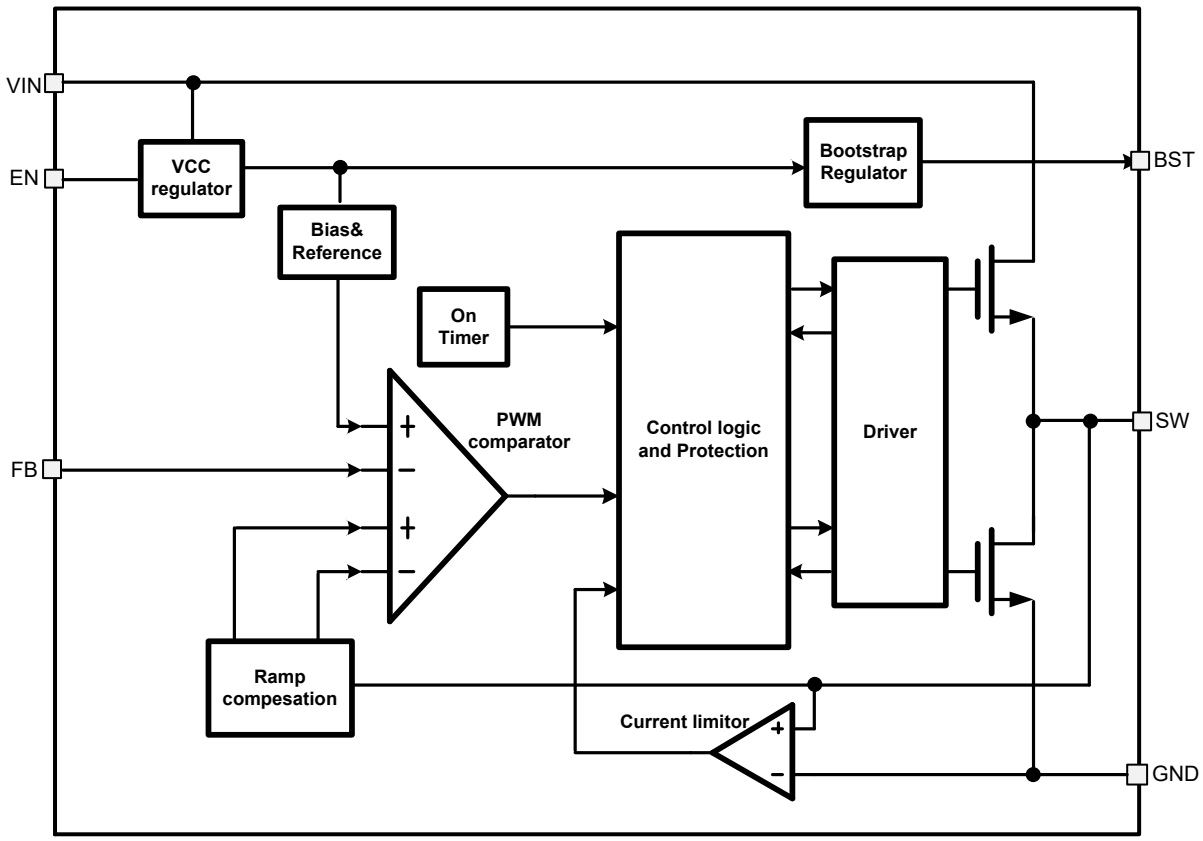



Figure 6. Quiescent Current Vs. Temperature

## FUNCTIONAL BLOCK DIAGRAM




 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

# OPERATION

### Adaptive On-time Control

The SCT2230 device is 4.2-17V input, 3A output, synchronous step-down converters with internal power MOSFETs. Adaptive constant on-time (ACOT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one shot time ON-time period. The one shot time is calculated by the converter's input voltage (VIN) and the output voltage (VOUT) cycle-by-cycle based to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. SCT2230 turns off high-side MOSFET after the fixed on time and turns on the low-side MOSFET. SCT2230 turns off the low-side MOSFET once the output voltage dropped below the output regulation, the one-shot timer then reset and the high-side MOSFET is turned on again. The on-time is inversely proportional to the input voltage and proportional to the output voltage. It can be calculated using the following equation (1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_S} \quad (1)$$

Where:

VOUT is the output voltage.
VIN is the input voltage.
fs is the switching frequency.

After an ON-time period, the regulator goes into the OFF-time period. The OFF-time period length depends on VFB in most cases. It will end when the FB voltage decreases below 0.8V, at which point the ON-time period is triggered. If the OFF-time period is less than the minimum OFF time, the minimum OFF time will be applied, which is around 200ns typical.

### Power Saving Mode (PSM)

The SCT2230 is designed with Power Save Mode (PSM) at light load conditions for high power efficiency. The regulator automatically reduces the switching frequency and extends Toff while no Ton changing during the light load condition to get high efficiency and low output ripple. As the output current decreases from heavy load condition, the inductor current decreases as well, eventually nearing zero current, this is the boundary between CCM and DCM. The low side MOSFET is turned off when the inductor current reaches zero level. The load is provided only by output capacitor, when FB voltage is lower than 0.8V, the next ON cycle begins. The on-time is the minimum on time that benefits for decreasing VOUT ripple at light load condition. When the output current increases from light to heavy load the switching frequency increases to keep output voltage. The transition point to light load operation can be calculated using the following equation (2):

$$I_{LOAD} = \frac{V_{IN} - V_{OUT}}{2L} \times T_{ON} \quad (2)$$

Where:

TON is on-time

### VIN Power

The SCT2230 is designed to operate from an input voltage supply range between 4.2V to 17V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 10uF may be required in addition to the local ceramic bypass capacitors.

© 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

### Under Voltage Lockout UVLO

The SCT2230 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.9V with VIN rising and shutdown threshold is 3.6V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

### Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.18V/rise), the SCT2230 enables all functions and the device starts soft-start phase. The SCT2230 has the built in 2ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 6.8uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 9. The resistor divider R3 and R4 are calculated by equation (3) and (4).

EN pin is a high voltage pin, and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

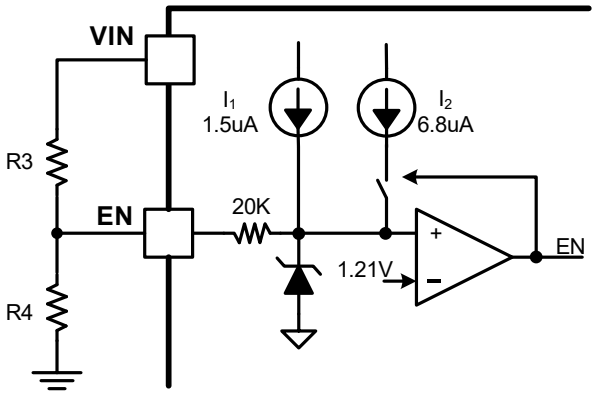



Figure 7. Adjustable VIN UVLO

$$R3 = \frac{V_{Start}\left(\frac{V_{ENF}}{V_{ENR}}\right) - V_{Stop}}{I_1\left(1 - \frac{V_{ENF}}{V_{ENR}}\right) + I_2} \quad (3)$$

$$R4 = \frac{R_3 \times V_{ENF}}{V_{Stop} - V_{ENF} + R_3(I_1 + I_2)} \quad (4)$$

Where:

- Vstart: Vin rise threshold to enable the device
- Vstop: Vin fall threshold to disable the device

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

- $I_1$=1.5uA
- $I_2$=6.8uA
- $V_{ENR}$=1.18V
- $V_{EMF}$=1.1V

**Over Current Protection (OCP) and Hiccup Mode**

In each switching cycle, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. When the voltage between GND pin and SW pin is lower than the over current threshold voltage, the OCP will be triggered and the controller keeps the OFF state. A new switching cycle will begin only when the measured voltage is higher than limit voltage. If output loading continues to increase, output will dropped below the UVP, and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup waiting time and restart normally after 7 cycles' soft-start period.

**Bootstrap Voltage Regulator**

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.2V rising and hysteresis of 200mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.2V, BST UVLO occurs. The SCT2230 intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

**Thermal Shutdown**

Once the junction temperature in the SCT2230 exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 140°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

© 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

# APPLICATION INFORMATION

## Typical Application

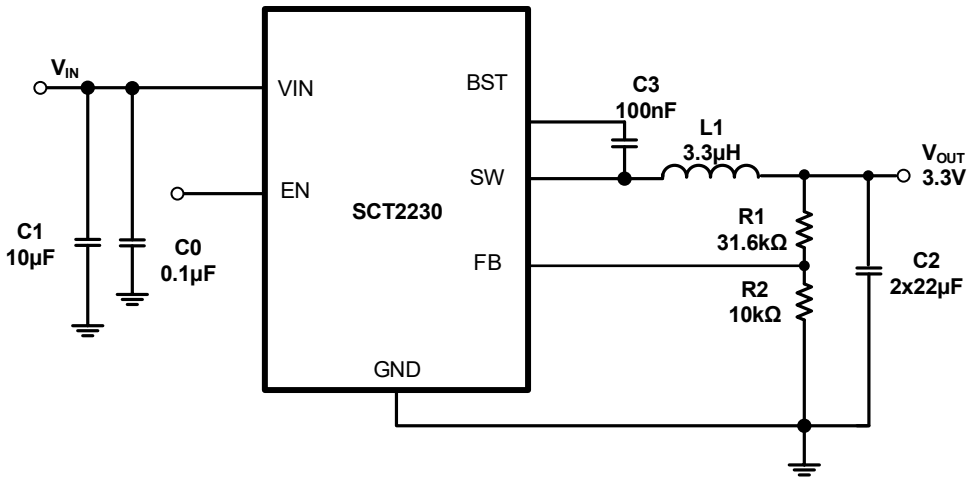



**Figure 8. 12V Input, 3.3V/3A Output**

**Design Parameters**

| Design Parameters | Example Value |
|---|---|
| Input Voltage | 12V |
| Output Voltage | 3.3V |
| Output Current | 3A |
| Switching Frequency | 750kHz |

### Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor anda0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2230.

Use Equation (5) to calculate the input voltage ripple:

$$\Delta V_{IN} = \frac{I_{OUT}}{C_{IN} \times f_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (5)$$

Where:

- $C_{IN}$ is the input capacitor value
- $f_{sw}$ is the converter switching frequency
- $I_{OUT}$ is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage

ripple less than 100mV. Generally, a 25V/10uF input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

**Inductor Selection**

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and buck converter efficiency. The inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maxim load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (6).

$$L_{INDMIN} = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times K_{IND} \times I_{OUT} \times f_{SW}} \quad (6)$$

Where:

- $K_{IND}$ is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, $I_{LPEAK}$, is calculated as in equation (7).

$$I_{LPEAK} = I_{OUT} + K_{IND} \times \frac{I_{OUT}}{2} \quad (7)$$

Set the current limit of the SCT2230 higher than the peak current $I_{LPEAK}$ and select the inductor with the saturation current higher than the current limit. The inductor's DC resistance (DCR) and the core loss significantly affect the efficiency of power conversion. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Table 1 lists recommended inductors for the SCT2230. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor 744325330 is used on SCT2230 evaluation board.

**Table 1. Recommended Inductors**

| Part Number | L (uH) | DCR Max (mΩ) | Saturation Current/Heat Rating Current (A) | Size Max (LxWxH mm) | Vendor |
|---|---|---|---|---|---|
| 744325330 | 3.3 | 5.9 | 15 | 10.5x10.5x4.7 | Wurth Electronik |

© 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

### Output Feedback Resistor Divider Selection

The SCT2230 features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure 8. Use equation (8) to calculate the resistor divider values.

$$R_1 = \frac{(V_{OUT} - V_{ref}) \times R_2}{V_{ref}} \quad (8)$$

**Table 2. Recommended Component Selections**

| Output Voltage (V) | SCT2231 R1 (kΩ) | R2 (kΩ) | L (μH) | C1 (μF) | C2 (μF) | C3 (nF) |
|---|---|---|---|---|---|---|
| 1.2 | 4.99 | 10 | 1.5 | 10 | 2 x 22 | 100 |
| 1.5 | 8.66 | 10 | 1.5 | 10 | 2 x 22 | 100 |
| 1.8 | 12.4 | 10 | 2.2 | 10 | 2 x 22 | 100 |
| 2.5 | 21.5 | 10 | 2.2 | 10 | 2 x 22 | 100 |
| 3.3 | 31.6 | 10 | 3.3 | 10 | 2 x 22 | 100 |
| 5.0 | 52.3 | 10 | 3.3 | 10 | 2 x 22 | 100 |

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

## Application Waveforms

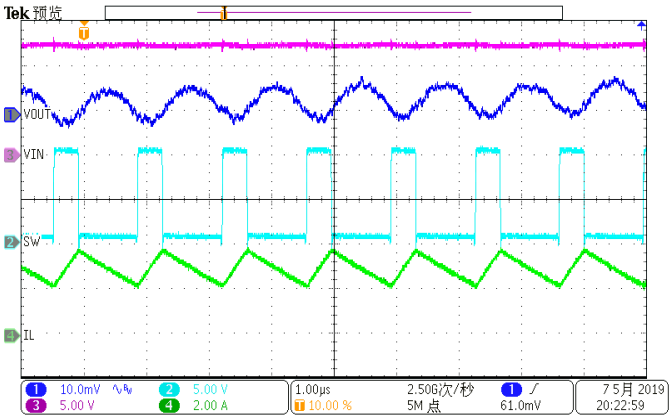



**Figure 9. SW node waveform and Output Ripple**
**VIN=12V, IOUT=3A**

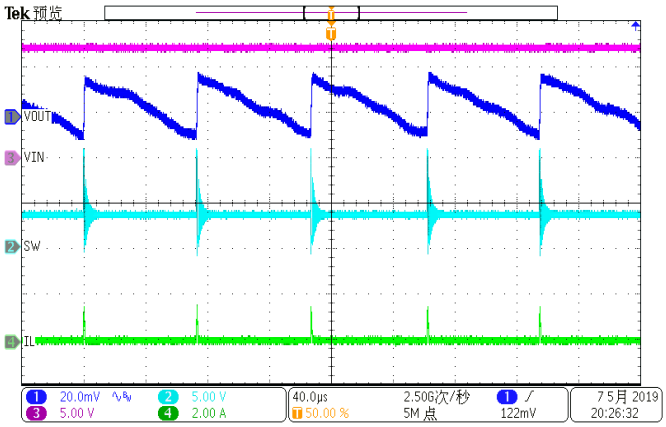



**Figure 10. SW node Waveform and Output Ripple**
**VIN=12V, IOUT=10mA**

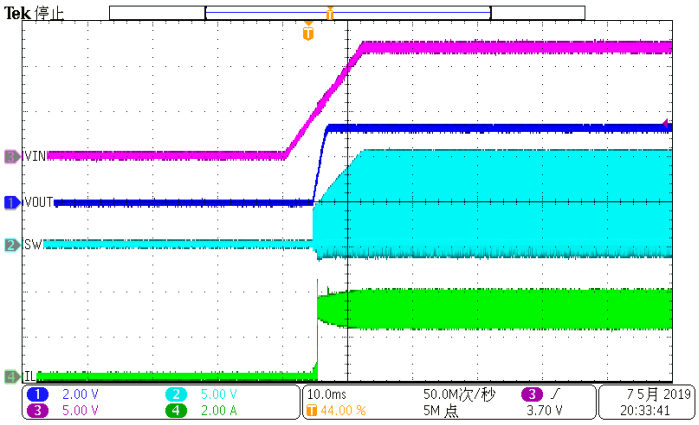



**Figure 11. Power Up**
**VIN=12V, VOUT=3.3V, IOUT=3A**

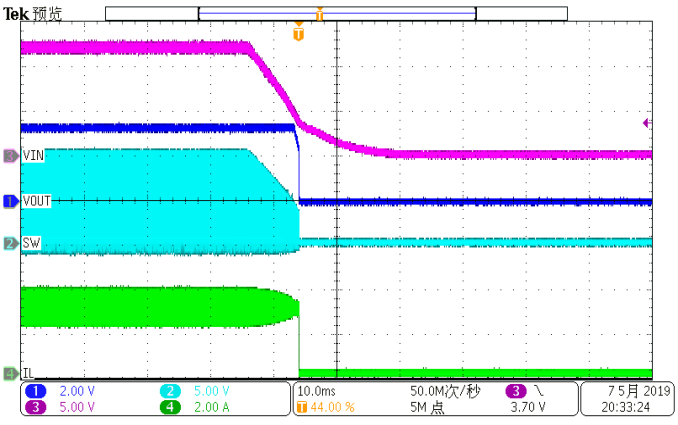



**Figure 12. Power Down**
**VIN=12V, VOUT=3.3V, IOUT=3A**

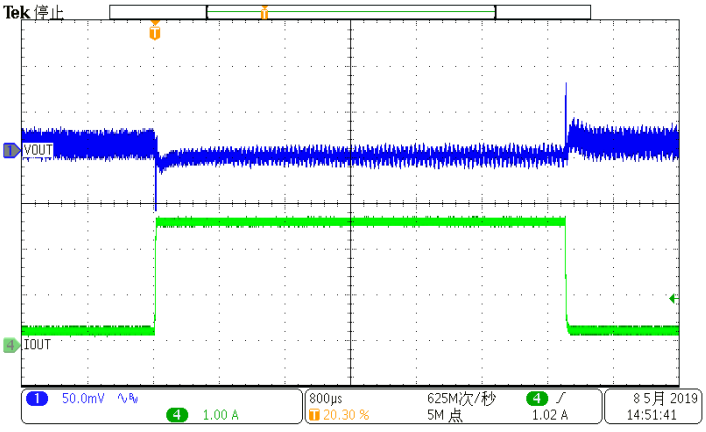



**Figure 13. Load Transient**
**VOUT=3.3V, IOUT=0.3A to 2.7A, SR=250mA/us**

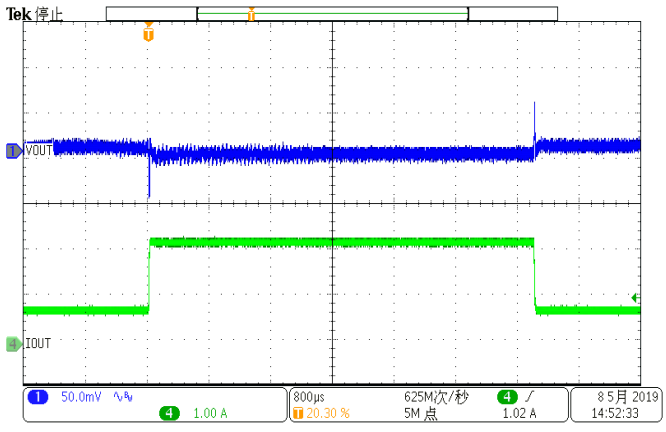



**Figure 14. Load Transient**
**VOUT=3.3V, IOUT=0.75A to 2.25A, SR=250mA/us**

© 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

### Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 15 is the recommended PCB layout of SCT2230.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

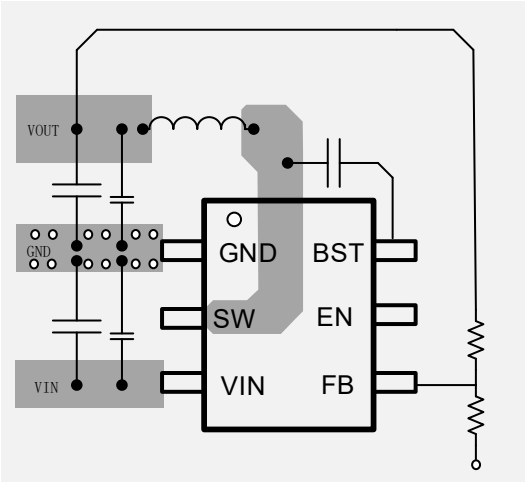



**Figure 15. PCB Layout Example**

### Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$ . The maximum-power-dissipation limit is determined using Equation (9).

$$P_{D(MAX)} = \frac{125 - TC_A}{R_{\theta JA}} \quad (9)$$

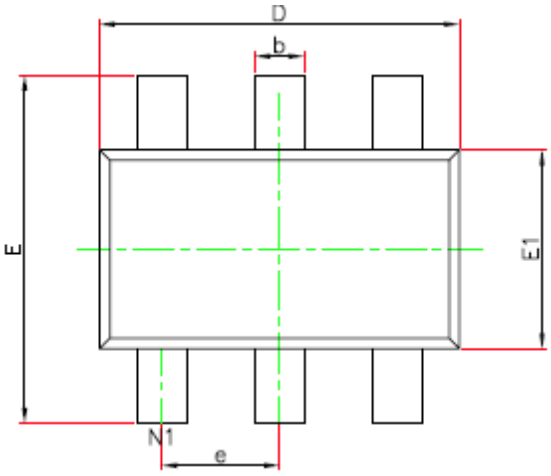
where

- $T_A$ is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the Thermal Information table.

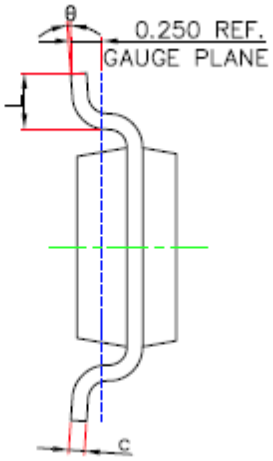
The real junction-to-ambient thermal resistance $R_{\theta JA}$ of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

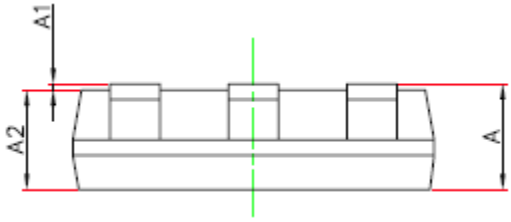
## PACKAGE INFORMATION (TSOT23-6L)




TSOT23-6L TOP VIEW




TSOT23-6L BOTTOM VIEW




TSOT23-6L SIDE VIEW

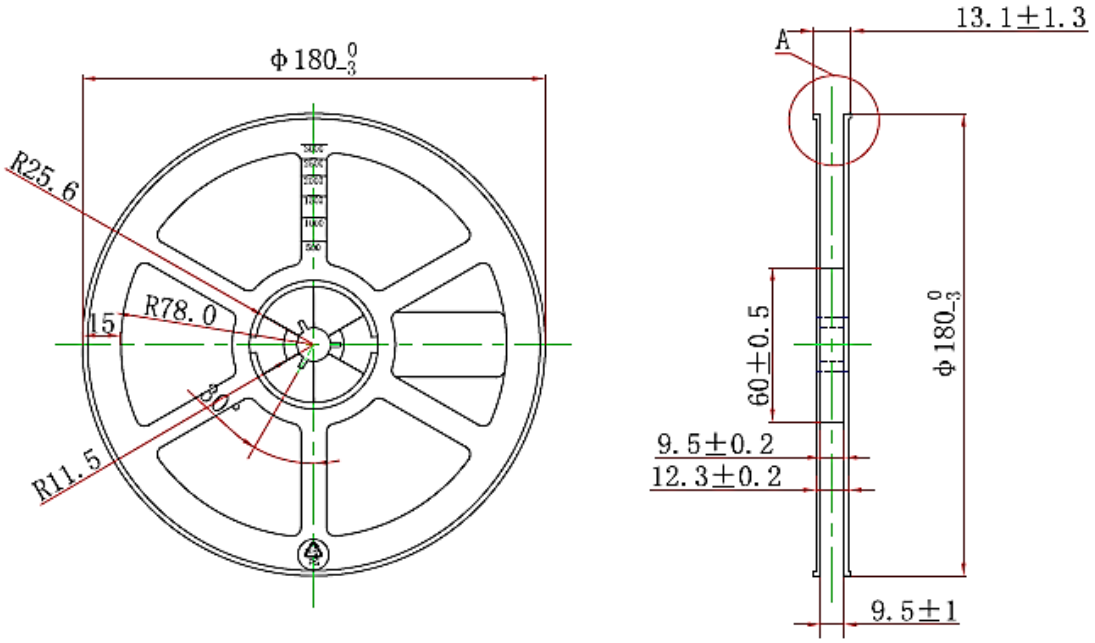
| SYMBOL | Unit: Millimeter | | |
|---|---|---|---|
| | MIN | TYP | MAX |
| A | ------- | | 1.10 |
| A1 | 0.000 | | 0.10 |
| A2 | 0.70 | | 1.00 |
| D | 2.85 | | 2.95 |
| E | 2.65 | | 2.95 |
| E1 | 1.55 | | 1.65 |
| b | 0.30 | | 0.50 |
| c | 0.08 | | 0.20 |
| e | 0.95(BSC) | | |
| L | 0.30 | | 0.60 |
| ɵ | 0° | | 8° |

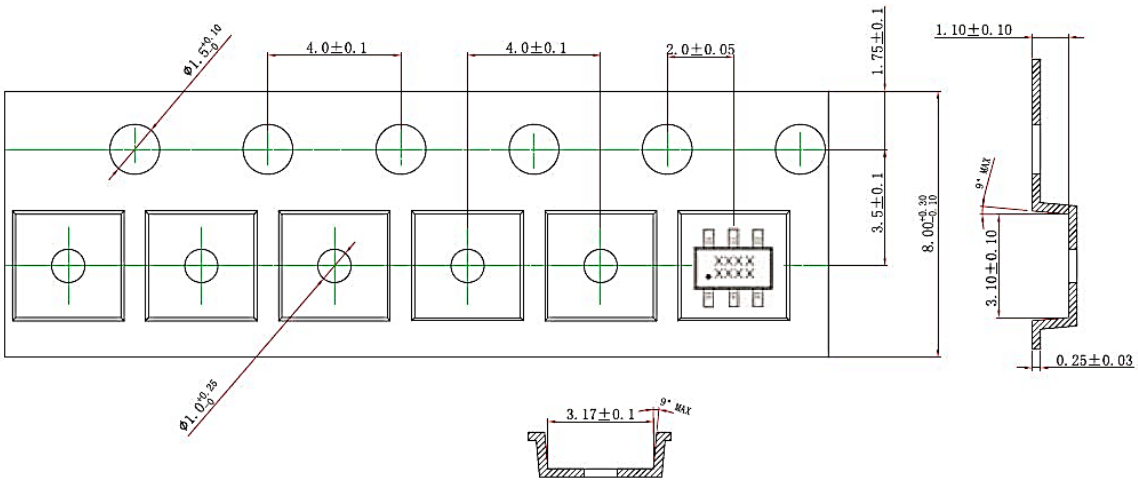
**NOTE:**

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

© 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

## TAPE AND REEL INFORMATION (TSOT23-6L)




**Feeding Direction**

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved